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Yi-Chung Chen, Hai Li, Wei Zhang, Robinson E. Pino

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Polytechnic Institute of NYU
2 MetroTech Center
Brooklyn, NY 11201

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14. ABSTRACT
For its simple structure, high density and good scalability, the resistive random access memory (RRAM) has emerged as one of the promising candidates for large data storage in computing systems. Moreover, building up RRAM in a three dimensional (3D) stacking structure further boosts its advantage in array density. Conventionally, multiple bipolar RRAM layers are piled up vertically separated with isolation material to prevent signal interference between the adjacent memory layers. The process of the isolation material increases the fabrication cost and brings in the potential reliability issue. To alleviate the situation, we introduce two novel 3D stacking structures built upon bipolar RRAM crossbars that eliminate the isolation layers. The bi-group operation scheme dedicated for the proposed designs to enable multi-layer accesses while avoiding the overwriting induced by the cross-layer disturbance, is also presented. Our simulation results show that the proposed designs can increase the capacity of a memory island to 8K-bits (i.e., 8 layers of 32 x 32 crossbar array) while maintaining the sense margin in the worst-case configuration greater than 20% of the maximal sensing voltage.

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Resistive memory, RRAM, 3D stacking, crossbar, bipolar operation

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3D-HIM: A 3D High-density Interleaved Memory for Bipolar RRAM Design

Yi-Chung Chen & Hai Li
Dept. of ECE
Polytechnic Institute of NYU
Brooklyn, NY, USA
Email: ychen33@student.poly.edu, hli@poly.edu

Wei Zhang
School of Computer Engineering
Nanyang Technological University
Singapore
Email: zhangwei@ntu.edu.sg

Robinson E. Pino
Advanced Computing
Air Force Research Laboratory
Rome, NY, USA
Email: robinson.pino@rl.af.mil

***Abstract*—Because of its simple structure, high density and good scalability, resistive random access memory (RRAM) is expected to be a promising candidate to substitute traditional data storage devices, *e.g.*, hard-disk drive (HDD). In a conventional three-dimensional (3D) bipolar RRAM design, an isolation layer is inserted between two adjacent memory layers. The fabrication of the isolation layer introduces the extra process complexity, increases fabrication cost, and causes some potential reliability issues. In this paper, we propose a 3D High-density Interleaved Memory (3D-HIM) design for bipolar RRAM, which can eliminate the need for forming isolation layers and further improve the density of the memory island. Meanwhile, we propose a Bi-Group Operation Scheme for 3D-HIM to access multiple cells among multiple layers and to avoid unexpected overwriting. The simulation results show that the proposed design is promising for a 3D stacking RRAM application with acceptable operation margin for a $32 \times 32 \times 8$ array in a memory island. The sensing margin degradation and programming bias confine the size of the array due to sneak path conducting currents. We diminish impact of sneak path conducting current by applying a high $\mathrm{R_{on}}$ RRAM device which can be achieved by a small-scale RRAM device.**

I. Introduction

When the conventional memory technologies, *e.g.*, SRAM, DRAM and Flash, are approaching their physical limitations, the rapidly increasing technology difficulties and fabrication costs force researchers to look for replacements [1]. In recent years, many emerging nonvolatile memories have been prototyped and utilized. Among them, the resistive random access memory (RRAM) has become a good candidate to substitute the traditional data storage technologies (*e.g.*, hard disk drive and flash memory) for its high density, low power consumption, and good scalability [2].

Three-dimensional (3D) stacking that builds up multiple memory layers vertically is an efficient way for density improvement. Conventionally, there is an isolation layer between two adjacent memory layers in order to avoid the malfunctions caused by the signal interference when simultaneously accessing multiple memory layers [3]. Manufacturing the isolation layers could introduce potential reliability issues, such as the melting (or even destruction) of metal interconnects during the annealing step. To prevent this from happening, a low thermal budget process, e.g., undoped Methylsilsesquioxane (MSQ) Spin-on-Glass (SOG) technology [4], is required, which could significantly increase the process complexity and the fabrication cost [5].

To obtain a high memory density while relaxing the requirements for process technology, we propose a new 3D High-density Interleaved Memory (3D-HIM) technique for bipolar RRAM devices. The proposed 3D-HIM can form the 3D memory structure without any isolation layers. Meanwhile, we can read or write multiple cells simultaneously on different memory layers to obtain a high throughput.

The key of the proposed design is to have two types of memory layers: one with the original memory stack and the other deposited in the reversed order. A memory island can be formed by applying these two structures to odd and even layers alternately and by sharing the electrodes and interconnection metal wires between two adjacent layers.

Our simulations show that 3D-HIM can function properly for a $32 \times 32 \times 8$ memory island. The minimal sensing margin is $\sim 20\%$ of the maximal sensing voltage, which can be sensed out by the peripheral circuit. In the paper, we also discuss and explore the design implications, such as the impacts of sneak path, and crossbar array size.

The rest of the paper is organized as follows: Section II gives a preliminary introduction on the RRAM device and crossbar array. Section III summarizes the previous work on 3D bipolar RRAM design and analyzes the process difficulties. Section IV explains the design concept of 3D-HIM and its read/write operations. Section V presents our simulation results and discusses the design implication to circuit design. At the end, Section VI concludes the paper.

II. RRAM and Crossbar Array

The resistive random access memory (RRAM) can be realized by many different materials based on the different storage mechanisms. All of these materials fall into only two operation types – *unipolar* switching and *bipolar* switching. Within this context, unipolar operation executes the programming/erasing by using short/long pulses, or by using high/low voltage with the same voltage polarity. In contrast, bipolar switching is executed with short pulses with opposite voltage polarity for programming and erasing [6]. Because bipolar device benefits from switching speed and power consumption in *RESET* (erase) operation [7], we target mainly on 3D RRAM structures with bipolar switching devices in this work. Material Cu-$\mathrm{Ge_{0.3}Se_{0.7}}$-$\mathrm{SiO_2}$-Pt [8] is used for demonstration. Please note that the proposed design concept can be easily extended to the other bipolar RRAM devices.

Figure 1(a) illustrates the structure of Cu-$\mathrm{Ge_{0.3}Se_{0.7}}$-$\mathrm{SiO_2}$-Pt [8]. It is a programmable metallization cell device formed in a sandwich structure with heterogeneous solid metal electrodes

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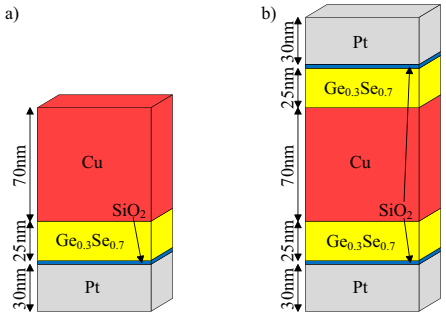

Fig. 1. (a) Structure of Cu-$Ge_{0.3}Se_{0.7}$-SiO_2-Pt. (b) The complementary cell structure.

at two poles. One pole is relatively inert Pt (called as the bottom electrode, or BE), the other is electro-chemically active Cu (called as the top electrode, or TE). A thin electrolyte film composed of ternary glass $Ge_{0.3}Se_{0.7}$ with added dissolved active metal Cu is placed between two electrodes. SiO_2 is used as a buffer layer to improve the endurance in the electrolyte [9]. The $Ge_{0.3}Se_{0.7}$ and SiO_2 are the places where the resistance changing happens.

For convenience, here we define R_{on} and R_{off} as the resistance value at the low resistance state (LRS) and at the high resistance state (HRS), respectively. The R_{off}/R_{on} is an important device parameter. In general, a high R_{off}/R_{on} is helpful to differentiate the LRS and HRS in the design.

When a negative bias is applied to the BE during a *SET* operation (that is, the device changes to the LRS), the dissolving Cu reacts with Se in electrolyte compound to form cation conductors which form a "filament" between two electrodes for electron transportation. As a result, the resistance between two electrodes is dramatically reduced. To *RESET* a cell (to change the device to the HRS), a positive bias can be applied on the BE to remove the random dissolving Cu from Cu-Ge-Se compound filament. The resistance becomes relatively high once the filament disappears in the electrolyte [9].

Crossbar array is widely used in the RRAM design for its simple structure and high density. Crossbar was firstly initiated and demonstrated in a telecommunication switching system, which contained two sets of wires and switches at cross points. Signal routing is controlled by properly selecting switches. In the nanometer-scale high-density memory design, the similar structure is maintained – a storage element is placed at each cross point of two sets of metal wires [10]. Theoretically, we can achieve the smallest memory cell area $4F^2$ by using crossbar array structure, where F is the minimum feature size [6].

Very recently, Linn *et al.* proposed a complementary RRAM cell structure, which is made of two anti-serial RRAM devices as illustrated in Figure 1(b) [11]. In such a complementary structure, at least one of the two RRAM devices exhibits the HRS under all the possible operation conditions. The existence of HRS can dramatically reduce the impact of sneak pathes. However, any single data recording has to be associated with a multi-step write procedure which requires careful and complex operation configuration. This brings in severe issues, such as power consumption and device reliability. Moreover, considering that each memory cell has includes two complementary RRAM devices, the memory capacity is only half of the conventional design.

III. Related Work

Simply stacking multiple memory layers vertically is a common way to construct 3D design with bipolar RRAM devices [12]. Each memory layer has its own set of storage elements and interconnects. An isolation layer is inserted between two neighboring layers to prevent the signal interference. Recently, an improved design was proposed by Kugeler *et al.*, in which word lines (WLs) between two memory layers can be shared [13]. The two memory layers sharing the same WLs can be accessed and programmed simultaneously. However, bit lines (BLs) cannot be shared, and hence, the manufacturing of isolation layers are still needed.

SOG with MSQ *etc.* materials can be used to form isolation layers. However, there are some critical difficulties from a process development point of view, including device degradation due to thermal processing [14], misalignment of vias due to SOG [15], poor adhesion of SOG material [4], and heat accumulation because of the low conductivity of the isolation material [14][16]. Consequently, a 3D memory design excluding isolation process can significantly benefit from lower fabrication cost and process complexity.

Previously, Jonson *et al.* presented a bipolar multi-layered conductive metal oxide memory without isolation layer, but it can be applied only to one-time programming ROM applications [17]. Very recently, a new 3D design for bipolar RRAM with interleaved complementary memory layers named as 3D-ICML was proposed [18].

IV. 3D High-Density Interleaved Memory

A. The Proposed 3D-HIM Structure

Figure 2 illustrates the proposed 3D-HIM structure. For simplicity, only six memory layers are demonstrated. A crossbar array is utilized in each layer. The basic design concept of 3D-HIM is to employ complementary material stack structures, *i.e.*, the regular memory stack and the one with a reversed deposition order, to the memory cells in neighboring layers. For instance, all the memory cells of Layer 1 in Figure 2 use the regular deposition process (purple pillars), and those

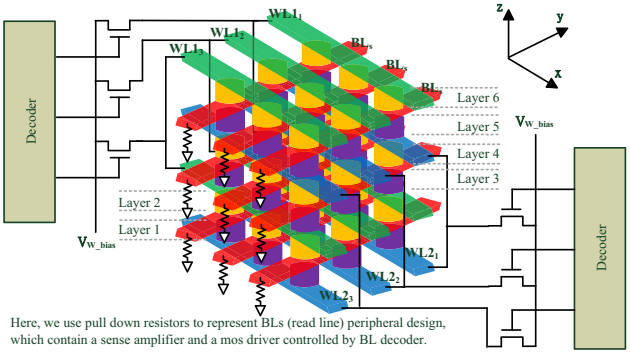

Fig. 2. 3D-HIM structure.

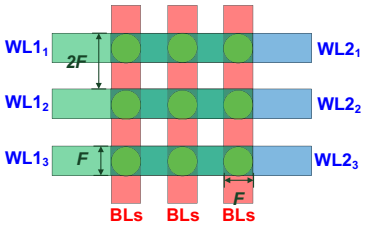

Fig. 3. Layout of 3D-HIM design.

of Layer 2 are made by reversing the deposition sequence (yellow pillars). The two types of memory stacks are applied to the odd and even layers alternatively. This process has been successfully demonstrated by Linn *et al.* and the memory cells made with regular and reversed depositions present the same device properties [11].

In the proposed design, memory devices and metal wires form a memory island without isolation layers. Any two adjacent memory cells at the same $x-y$ location are connected back to back, and hence, share the metal wire in between.

Some terms are defined to help understand the proposed structure and corresponding operations.

- Bitlines (BLs): A set of metal wires connected to TEs of RRAM devices, which route along the $y-$axis as shown in Figure 2.
- Wordlines (WLs): A set of metal wires connected to BEs of RRAM devices, which route along the $x-$axis. There are two sets of WLs, names as WL1 and WL2.
- WL1s and WL2s: We number the WL layer at the bottom of the 3D-HIM structure as '0' and continue counting the other WL layers from bottom to top. We define WL1s (WL2s) as those WL layers with odd (even) numbers.
- WL1$_i$GC and WL2$_j$GC: we name the group of memory cells connected to a given WL1$_i$ or WL2$_j$ as WL1$_i$GC (WL1$_i$ group cells) or WL2$_j$GC (WL2$_j$ group cells), respectively.

Totally, three sets of control signals, *i.e.*, BL, WL1 and WL2, are utilized. Each of them is responsible to the related operations to the memory layers above and below it.

B. Memory Density Improvement

Figure 3 illustrates the layout of a 3D-HIM from top view. The cell area is $A_{3D-HIM} = 4F^2$, which is the same as the cell size of the conventional crossbar array ($A_{conv} = 4F^2$). Note that for a 3D memory, its density is determined not only by the single memory cell area, but also by the the allowable number of memory layers. By sharing BEs and TEs between neighboring layers, 3D-HIM can reduce the overall number of conduction layers and remove isolation layers. For a given height of a 3D structure, which usually is a major limitation in fabrication process, more memory layers can be stacked up vertically. Thus, the memory capacity increases.

C. Memory Accesses in 3D-HIM

1) Bi-Group Operation Scheme: In 3D-HIM, there are two sets of group cells – WL1$_i$GC and WL2$_j$GC. Only one of them can be accessed at once during read or write operations. We called it as "Bi-Group Operation Scheme."

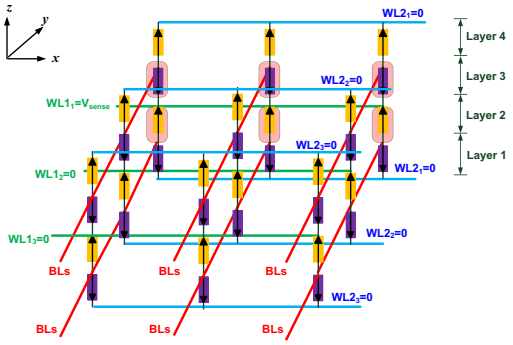

Fig. 4. Selected WL$_1$GC in read operation.

This scheme has several advantages: (1) It increases throughput by simultaneously accessing multiple memory cells within either WL1$_i$GC or WL2$_j$GC. (2) The unselected groups can be biased to ground and taken as the signal isolators. Thus, we can avoid the unexpected overwriting caused by the write operations on different memory layers. (3) The BLs are shared by the RRAM layers above the BLs, and below BLs. The peripheral circuitry connected to the BLs are also shared by two RRAM layers to reduce area cost. Furthermore, WL1 and WL2 can be driven from the opposite sides of the memory island as shown in Fig. 2 to distribute the layouts of peripheral circuitry.

2) Read Operation: To read out the stored data in a RRAM cell, we provide a sense voltage (V_{sense}) to the corresponding WL, and measure the current through the cell. To prevent the unexpected overwriting, V_{sense} should be much smaller than the threshold voltage of RRAM device. A sense amplifier is connected to the BL and shared by two group's cells WL1$_i$GC and WL2$_i$GC. Based on the Bi-Group Operation Scheme, only one group's cells can be sensed out at one time.

Fig. 4 shows an example of reading out the cells in WL1$_1$GC. Accordingly, WL1$_1$ is raised to V_{sense} and all the other WL1$_i$ are tied to 0 V. To prevent the disturbance from/to WL2 groups, all the WL2s are forced to 0 V. Similarly, the read operation of WL2$_j$GC on the $x-y$ plane can be accessed simultaneously (which is omitted here due to space restriction).

An active load (R_{sense}) is used at the end of BL to transfer current through the memory device to the input voltage of a sense amplifier $V_{R-sense}$. To simplify the evaluation of the read operation in this work, we apply a 100 Ω resistance (R_{sense}) as the input resistance of sense amplifier, and define the sensing margin (SM) by normalizing $V_{R-sense}$ with V_{sense}.

Assume that a 3D-HIM memory island has H memory layers, and each of them includes a $N \times N$ array. The capacity of such a memory island is $MC = N^2 \cdot H$ and the read bandwidth is $BW_{Read} = N \cdot H/2$.

3) Write Operation: As we state above, Bi-Group Operation Scheme needs to be used in write operation to increase throughput and prevent unexpected overwriting. There are two possible write procedures – SET and RESET. Like all the bipolar RRAM crossbar design, these two procedures have to be separated because they require the opposite driving

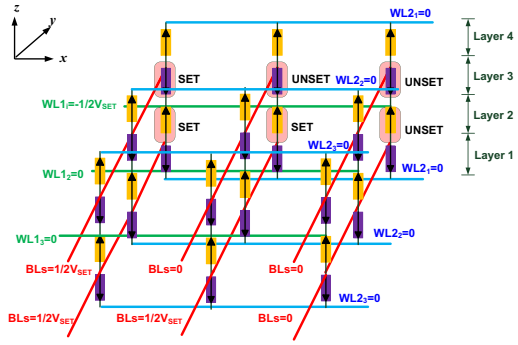

Fig. 5. Selected WL_1GC in SET operation.

polarities. In 3D-HIM, the cells that programmed at the same time must locate in the same group and have the same incoming value.

The driving conditions need to be carefully controlled to avoid unexpected overwriting caused by sneak paths and to minimize the total write current. The ideal bias voltages when performing SET and RESET are summarized in Table I. All the other WL1s, WL2s and BLs that are not related to the writing operation are forced to 0 V.

Fig. 5 illustrates an example of $WL1_1GC$ during a SET operation. For illustration purpose, we assume half of the cells in $WL1_1GC$ are in the SET procedure. $WL1_1$ are forced to $-0.5V_{SET}$, the BLs connected to the cells to be programmed are forced to $0.5V_{SET}$, and the unrelated control signals are set to 0 V. As shown in Fig. 5, a unselected cell within $WL1_1GC$ have only $0.5V_{SET}$ voltage drop across the cell, which is not big enough to change its content. The RESET procedure is similar to the SET in the example. The corresponding bias voltages are summaries in Table I. To save some space, we omitted the write operation of $WL2_jGC$ on the $x-y$ plane, which has the similar setup requirement.

The average write bandwidth of 3D-HIM is $BW = N \cdot H/4$, while the maximal write bandwidth could be $N \cdot H/2$ when all the cells in the given group are programmed to the same content.

V. Simulation Result & Discussion

We did simulations for the proposed 3D-HIM structure by using Spectre on Cadence CAD platform. The characteristic parameters of RRAM are summarized in Table II [19].

To be more realistic, we embedded interconnect resistance (IR) in the simulation model. The existence of IR on control signals can result in voltage drop and decreases the real driving voltage delivered to the target memory cells. Based on the DRAM interconnect requirement at $22nm$ technology node from ITRS 2009, we set IR per memory cell $R_{Interconnect} = 2.5\Omega$ [20]. Considering the limitations of back-end process,

TABLE I
Driving Conditions of Writing Operations

Data	Cell Group	Driving Conditions
LRS	$WL1_iGC$	WL1:$-0.5V_{SET}$, BL:$0.5V_{SET}$
LRS	$WL2_jGC$	WL2:$-0.5V_{SET}$, BL:$0.5V_{SET}$
HRS	$WL1_iGC$	WL1:$-0.5V_{RESET}$, BL:$0.5V_{RESET}$
HRS	$WL2_jGC$	WL2:$-0.5V_{RESET}$, BL:$0.5V_{RESET}$

TABLE II
Parameters of RRAM and 3D-HIM

Parameters	Value	Parameters	Value
V_{SET}	1.5 V	$R_{Interconnect}$	2.5 Ω
V_{RESET}	1 V	V_{sense}	0.1 V
R_{off}(HRS)	1 MΩ	R_{sense}	100 Ω
R_{on}(LRS)	5 kΩ		

we assume up to eight memory layers can be stacked up in 3D-HIM.

A. Impact of Data Pattern and Cell Location

1) Impact of Data Patterns: The effectiveness of read and write operations in 3D-HIM depends on the memory data pattern. To investigate the impact of data pattern, we divide all the cells in a memory island into three catalogs: the target cell, the cells along the driving path (i.e. WL1 or WL2), and all the other cells. Figure 6 shows an example of the $WL1_1GC$ in the sensing operation: the target cell highlighted in PURPLE, the cells along the driving path (WL1) highlighted in BLUE, and all the other cells not highlighted. Four data patterns can be introduced – "LL", "LH", "HH" and "HL". Here, the first letter stands for the status of the target cell ('L'=LRS, 'H'=HRS), and the second letter stands for the cells along driving path, either WL1s or WL2s.

Our work shows that the cells along the driving path and the rest cells dominate the SM rather than the target cell. The worst case happens when the driving path cells and the rest cells are all at LRS. In such situation, the conducted current from the sneak paths and leakage current are maximized. The corresponding data pattern are "LL" or "HL". The impact of data patterns to the SM in our design is further discussed in the next section.

2) Impact of Cell Location: The physical location of a cell could affect its operation scenario. For example, Fig. 7 illustrate a two-layer 3D-HIM in read operation of $WL1_1GC$. The driving current flows from the leftmost side of $WL1_1$ to the rightmost of the array along the x-axis. Due to interconnect resistance, the real voltages applied on the cells along $WL1_1$ are not same. The worst case scenario happens at the cell in the right corner (highlighted in RED) because it goes through the longest path from the driver to the sense circuitry. In the contrast, the cell located in the left corner (highlighted in

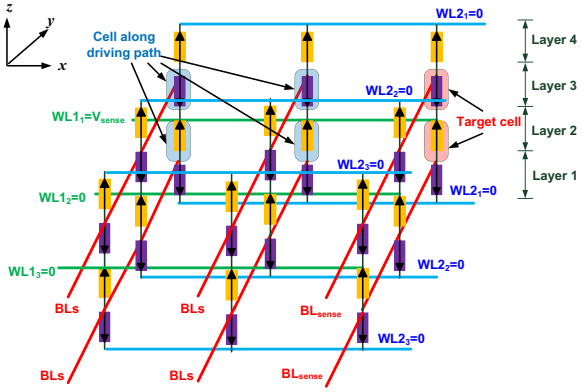

Fig. 6. Three catalogs of cells used for data patterns analysis.

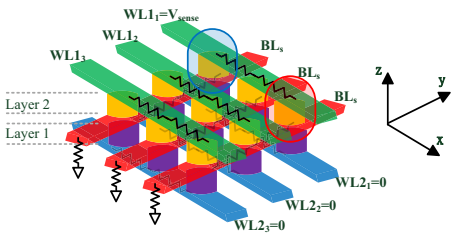

Fig. 7. Worst case and best case scenario of the cell locations.

BLUE) is affected least by the interconnect resistance, and hence, becomes the best situation.

Fig. 8 shows the SM difference between the worst scenario and the best scenario of cell locations with different data patterns in a four-layer 3D-HIM. As shown in the results, the impact of array size to the 'LL' pattern is much larger than the other patterns: the location difference incurs more than 10% SM difference. This is because the target cell at LRS suffers from high interconnect resistance and the other cells on sneak path at LRS sink a big portion of currents. To ease impact of location difference, RRAM of high $\mathrm{R_{on}}$ which suffers less impact of IR is promising for large scale array.

B. Read operation

Fig. 9 compares the SMs of conventional 3D RRAM and 3D-HIM under different memory parameters. The worst case scenario of cell location and data pattern is assumed in the simulation.

The SMs of a conventional 3D RRAM at different array sizes are shown in Fig. 9 by the BLUE curve. The BLACK curves demonstrate the SMs of a 3D-HIM with different layer numbers. The curves for 4-layers and 8-layers merged together. Compared to the conventional 3D RRAM, 3D-HIM loses $10 \sim 20\%$ in SM. This is because that the conventional 3D RRAM inserts a isolation layer between any two memory layers, hence, the SM is determined only by one crossbar array. The control signals (e.g., WLs) in 3D-HIM have to drive twice number of memory cells than the conventional design, which introduces more sneak paths. However, because of the interleaved design, stacking more layers in 3D-HIM only induces slight degradation on SM. The SM decreases obviously as the array size increases. For example, in a four-layer 32×32 3D-HIM, the SM is about 20%. When array size increases to 64×64, the SM significantly reduces to 3%, which means the status of memory cells are hard to be detected.

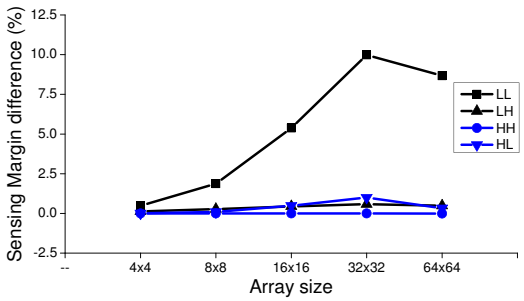

Fig. 8. SM difference by the cell locations and data patterns

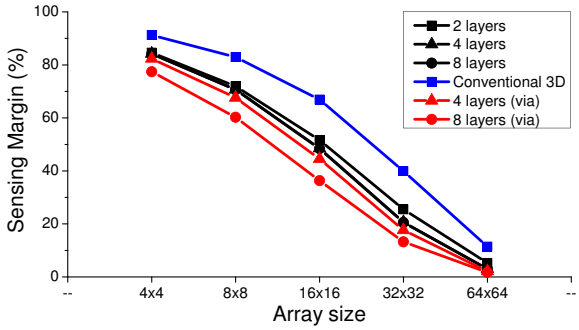

Fig. 9. SM of 3D-HIM

The small footprint of via could introduce a large resistance on the driving path, which incurs performance degradation in the upper layers. Based on ITRS 2009 – DRAM Interconnect technology requirements for $22nm$ technology [20], we approximate the via resistance as 14Ω. The RED lines in Fig. 9 shows the simulation results of 3D-HIM after including the impact of via resistance in small footprint.

Fig. 10 shows the composition of the sensing current under 'HL' pattern. As the array size increases, the percentage of the sneak path conducting current raises. In a four-layer 64×64 3D-HIM, the conducting current in the sneak path contributes 99% of the sensing current in 'HL' data pattern, which makes it hard to detect the correct memory status and reduces the SM significantly. To further increase the SM in 3D-HIM, we have to suppress sneak path current. By increasing $\mathrm{R_{on}}$ at LRS, the impact of sneak paths can be dramatically relieved. In Fig. 10, we compare the simulation results of $\mathrm{R_{on}}$=10kΩ with the results of using the original value $\mathrm{R_{on}}$=5kΩ. Increasing $\mathrm{R_{on}}$ to 10kΩ can eliminate 35% and 5% of the sneak path conducting current in a 16×16 and 64×64 array, respectively. Correspondingly, the sense margin of the 64×64 and 16×16 array improves to 11% and 20%, which increases the margin of the sense amplifier design of 3D-HIM. We can conclude the increasing sensing voltage of HL data pattern has significant impact to SM degradation. To suppress sneak path conducting current is a promising method to improve SM degradation.

C. Write operation

The cell location and data pattern also affect the write operations. The worst case happens at the same location and with the same data pattern as in the read operation. Due to space limitation, we only discuss the worst case scenario and follow the explanation for read operation.

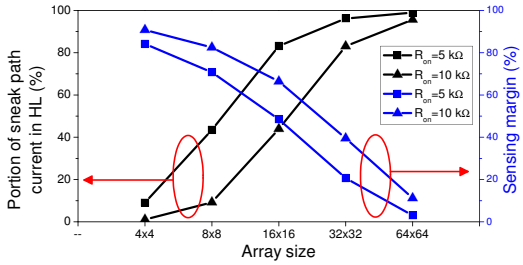

Fig. 10. Portion of sneak path conducting current in sensing current through $\mathrm{R_{sense}}$ and SM of four-layer 3D-HIM with various $\mathrm{R_{on}}$

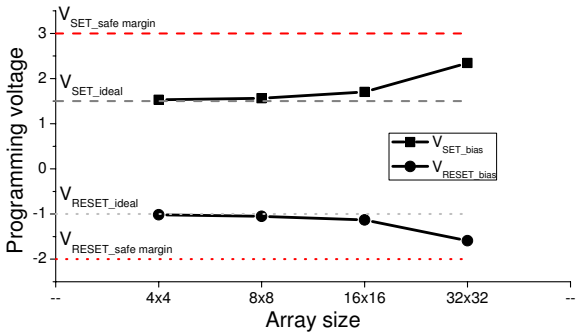

Fig. 11. Proper programming voltage

Enlarging array size of 3D-HIM increases the total IR in a driving path. To compensate the impact of the increasing voltage drop on IR and properly program the target cells, a higher bias between WLs and BLs (V_{SET} or V_{RESET}) is required. The corresponding simulation for a four-layer 3D-HIM with various array sizes is shown in Fig. 11.

The two dotted GRAY lines are the required SET and RESET voltages across a RRAM cell, which are exactly $V_{SET-bias}$ and $V_{RESET-bias}$ in the ideal condition without IR. However, the impact of IR cannot be ignored in a real design and it results in the increase of programming voltages as array size increases as demonstrated by the BLACK curves. The dotted RED lines constrain the safe margins of programming voltages, which double the range of the GRAY curves. If V_{SET} or V_{RESET} exceeds the safe margins, some unselected cells may be overwritten since their voltage drop are higher than the threshold. As a result, the proper programming voltage (BLACK curves) and safe programming margins (RED lines) confine the array size. Our simulation shows that the maximal allowable array size of 3D-HIM is 32×32 to satisfy the constraints in write operations.

VI. Conclusion

In this paper, we proposed a high density 3D stacking memory structure called 3D-HIM, which has advantages in geometric considerations without losing much performance. Its interleaved structure helps to maintain sensing margin and proper programming voltage while suppressing impact of sneak paths and leakage current. 3D-HIM can be fabricated by a simple process by forwarding and reversing the deposition sequence of RRAM materials alternatively. Intuitively, this structure can be utilized in any bipolar RRAM, especially when materials with a higher R_{on} is preferable. 3D-HIM is expected to be a promising 3D high density non-volatile memory system for future mass storage device.

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